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3-Level Neutral-Point Clamped Inverters Using Multi Carrier Pulse Width Modulation for FACTS Applications

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Abstracts

In this paper, a novel technique used to keep the voltage across the dc split capacitors of neutral point clamped inverter using multi carrier pulse width modulation and also compensate the reactive power. It can reduce the harmonics without any changes in inverter output. Multi carrier pulse width modulation is controlling the neutral point voltage at full modulation index. It require compensation loop because it does not deliver the natural voltage balancing. The voltage is balanced under all operating conditions. This results in smaller harmonics, but on the other hand it has more components and is more complex to control. In this paper, different three level inverter topologies and SPWM technique has been applied to formulate the switching pattern for three level inverter that Minimize the harmonic distortion at the inverter output. Simulation result has discussed.

Keywords: SPWM, THD, PWM.

Introduction

Numerous industrial applications have begun to require high power apparatus in the recent years. Some motor drives and utility applications require medium voltage and megawatt power [3][12][15]. For a medium voltage grid, it is bothersome to connect only one power switch directly. A structure of multi-level inverter is introduced as high power and medium voltage. A multilevel inverter not only accomplishes high power applications and also enable for renewable energy sources such as wind, solar and biomass energy. However, a multilevel inverter to reach high power is to use a series of power semiconductor switches with several dc sources to implement the power conversion by staircase waveform. Capacitors, batteries and renewable energy voltage sources can be recycled s multiple d sources. A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The main topology of multilevel inverters is diode clamped inverter, flying capacitor and cascaded H- bridge inverter. Neutral Point Clamped Inverter is more preferred than other topology. Nowadays Neutral point clamped inverter have important development to achieve high power with dissimilar voltage level and also deliver more advantages than conventional inverter. Such as, low switching losses, high power quality of waveform without certain order harmonics and reduced output dv/dt. But these features are obtained when the voltage across the capacitor is balanced under different working conditions.

Fig 1.0 Main power stack characteristics

Multilevel inverter topologies

The basic three types of multilevel topologies used are [10][4]:

(1) Diode clamped multilevel inverters

(2) Flying capacitors multilevel inverter or capacitor clamped multilevel inverter

(3) Cascaded inverter with separate DC sources. A .Diode Clamped Multilevel Inverters The diode clamped

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multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m level diode clamp inverter needs (m-1) capacitors on the dc bus.

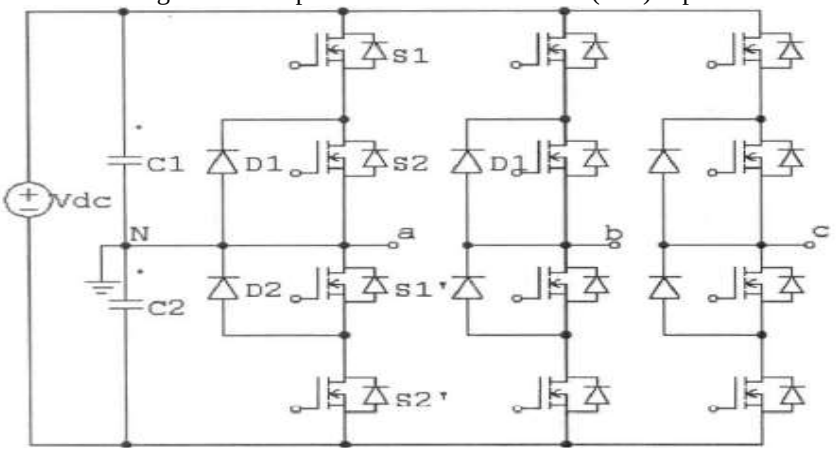

Fig 2.0 Diode Clamped Three Level Inverter

A. Flying Capacitor Multilevel Inverter

It uses ladder structures of dc side capacitors where the voltage on each capacitor differs from that of the next capacitor. To generate m- level staircase output voltage, (m-1) capacitors in the dc bus are needed. The size of the voltage increment between two capacitors determines the size of the voltage levels in the output wave.

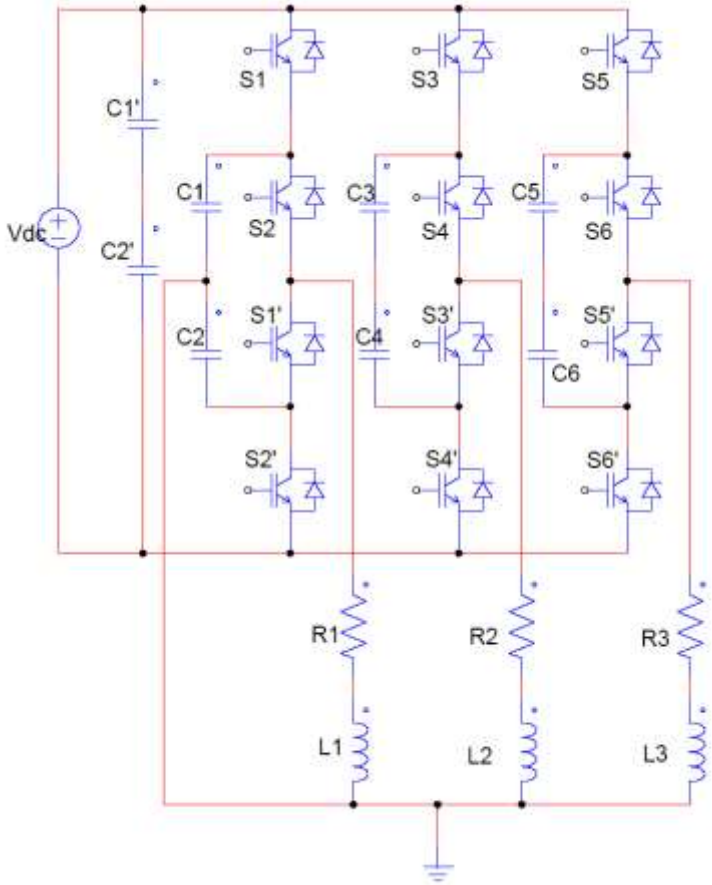

Fig. 2 Flying Capacitor Three Level Inverter

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System configuration

The proposed three level inverter with RL load, which consists of voltage source inverter. The inverter model connected to the RL load is controlled to produce the staircase voltage and sinusoidal current. Three levels PWM based on constant carrier frequency for three level inverter systems is proposed to reduce the harmonic contents in the output voltage and decrease the voltage rating of the power device.

Analysis of the average current contribution to the midpoint and an average mode

This section begins by analyzing the current contribution to the midpoint for the three voltage balancing techniques explained in the previous section. Subsequently, a sensitivity analysis for different modulation indexes and phase-shift angles is performed. Next, a small signal averaged model of the midpoint balance control loop, suitable for control design purposes, is proposed.

A. Analysis of the Current Contribution to the Midpoint

As already explained in the instantaneous duty ratio *d* of the portion of the phase input current that flows to the midpoint is defined as

$$d_K = \begin{cases} 1 + {}^{2v_K}/_{E} & \left({}^{-E}/_{2} \le v_K < 0\right) \\ 1 - {}^{2v_K}/_{E} & \left(0 \le v_K \le {}^{-E}/_{2}\right) \end{cases}$$

where *k = A, B, or C*

Consequently, the instantaneous contribution of any phase to the midpoint current is obtained by multiplying the duty ratio *dK* by the phase current (1)

$$i_{M-K} = d_K\, i_K\,.$$

Since the voltage drift of the midpoint is a comparatively slower varying process than the instantaneous voltage ripple present in the dc bus, the effectiveness of the midpoint voltage control can be evaluated by considering the mean dc midpoint current over an entire line period *T*. This is calculated in a straightforward manner as

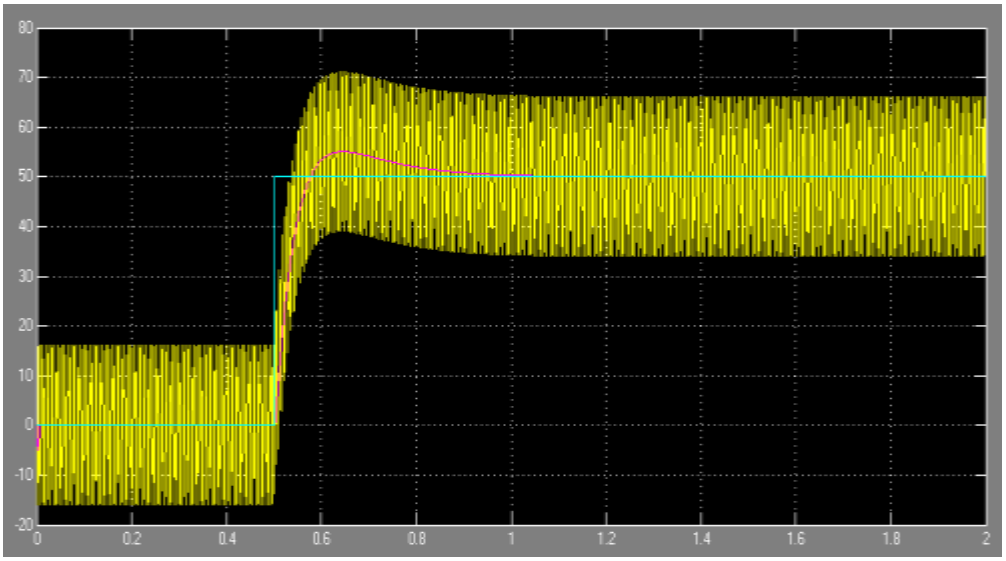
$$\bar{i}_{M-K} = \frac{1}{T}\int_0^T i_{M-K}\,dt$$

$$\bar{i}_M = \bar{i}_{M-A} + \bar{i}_{M-B} + \bar{i}_{M-C}$$

$$= \frac{1}{T}\int_0^T (i_{M-A} + i_{M-B} + i_{M-C})\,dt.$$

The effect that the injection of a negative sequence second harmonic, sinusoidal sixth harmonic and squared sixth harmonic, have on the midpoint current can be visually seen by looking at the waveforms

Results



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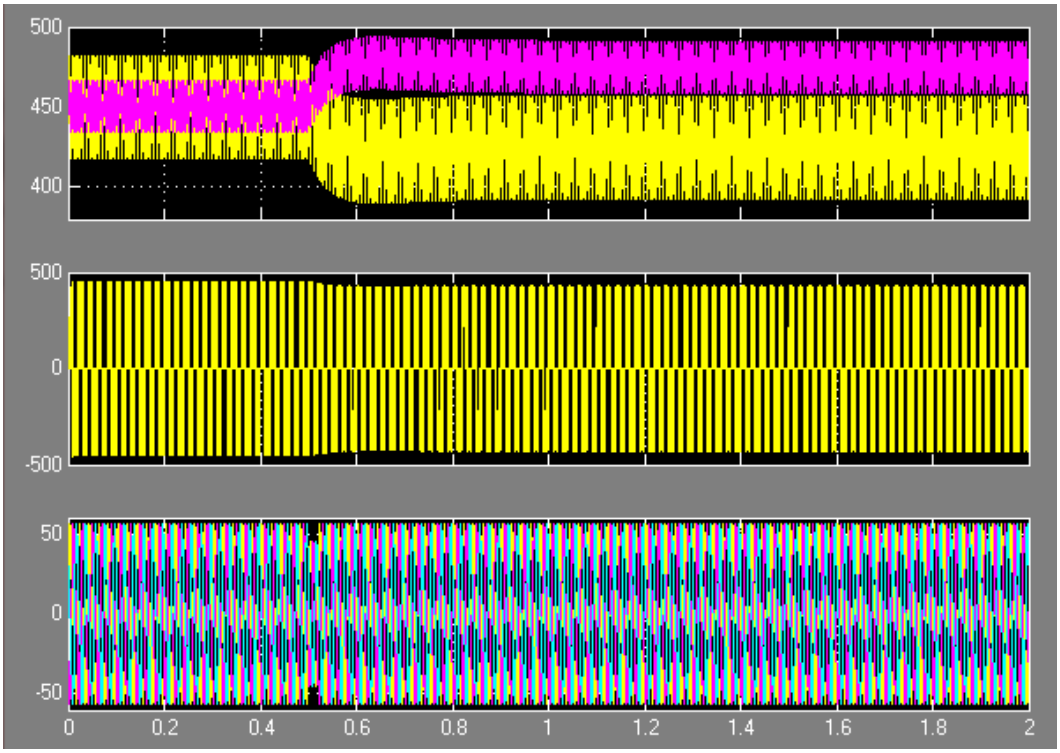

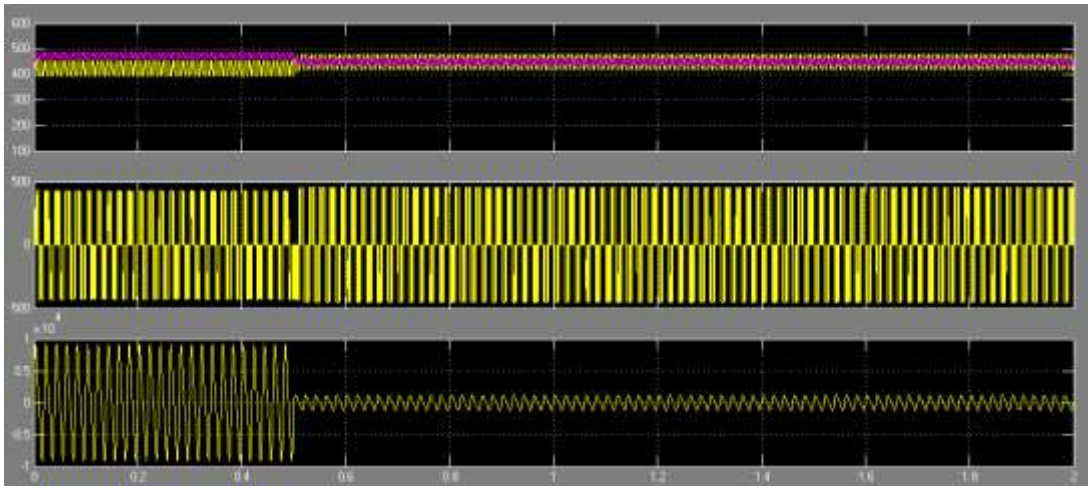

Conclusion

The simulation of the inverters namely conventional three and two level inverter was carried using sinusoidal pulse width modulation (SPWM) .it has shown that decrease in voltage and current THD in moving from two level inverter to three level inverter. This paper briefly explains theory of sinusoidal pulse width modulation (SPWM) for two and three level inverter and performance of both inverters was tested using RL load. It has shown that load current for three level inverter are much more sinusoidal and improvement in the line current waveform and decrease in the THD from two level to three level inverter and decrease in the THD as the frequency is increased.

References

1. J. S. Lai and F.Z. Peng "Multilevel Converters – A new breed of power converters" IEEE Trans. Ind Applicant , Vol. 32, May/June 1996.
2. Jose Roderiguez, Jih-Sheng Lai and Fang Zheng Reng, "Multilevel Inverters" A survey of topologies ,control, and applications ",IEEE Trans. On Ind.Electronics, vol No.[4], August 2002.

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Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 2.114

3. A. Nabae, I Takashashi, and H. Akagi, " A new neutral –point clamped PWM inverter," IEEE Trans. Ind Application Vol. No. IA-17,PP 518-523,Sept/oc 1981.
4. Novel Multilevel Inverter Carrier-Based PWM Methods, IEEE IAS 1998 Annual Meeting, St. Louis, Missouri, October 10-15, 1998, pp.1424-1431.
5. Multi Carrier PWM based Multi-Level Inverter for High Power Application, 2010 IJCA (0975-8887) Volume 1- No.9
6. Voltage-Balancing Compensator for a Carrier-Based Modulation in the Neutral-Point-Clamped Converter, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL.56, .NO2, FEBRUARY 2009
7. Harmonic Orientation of Pulse Width Modulation Technique in Multi-Level Inverters, POWER ENGINEERING AND ELECTRICAL ENGINEERING, VOLUME: 9, NUMBER: 1, 2011 MARCH.
8. A Carrier-Based PWM Strategy With the Offset Voltage Injection for Single-Phase Three-Level Neutral Point Clamped Converters, Wensheng Song, Xiaoyun Feng, and Keyue Ma Smedley, Fellow, IEEE.
9. A Comparative Study of Total Harmonic Distortion in Multi-Level Inverter Topologies, Journal of Information Engineering and Applications ISSN 2224-5782, Vol 2, No.3, 2012.
10. Performance Evaluation of Multi Carrier Based PWM Techniques for Single Phase Five Level H-Bridge Type FCMLI, IOSR, ISSN: 2250-3021 Volume 2, Issue 7(July 2012), pp 82-90.